REMARKS/ARGUMENTS

Applicants amended para. [0003] on pg. 2 of the Specification to correct a referenced patent number 5,426,761.

Applicants amended para. [0021] on pgs. 8-9 to remove a phrase.

1. Amended Claims 17-24 Comply with Sections 101 and 112, par. 2

The Examiner rejected claims 17-24 as directed to non-statutory subject matter (35 U.S.C. §101) on the grounds that the article of manufacture could cover "transmission" media, which the Patent Office regards as non-statutory.

Applicants traverse the basis for this finding because Applicants submit that signals and "transmission media" are statutory because they provide a tangible embodiment of code in a physical media of transmitted signals that may be transmitted and received and interpreted. Applicants submit that implementing or embedding code in transmission signals is as tangible as embedding code in magnetic transitions in a magnetic storage media, which the Patent Office recognizes is statutory and "tangible" subject matter.

Moreover, even if one could regard "transmission media" as intangible and non-statutory, the claims by definition cannot cover non-statutory subject matter so there is no need to amend them in their current form because the "article of manufacture" language also covers subject matter the Patent Office recognizes as "statutory", such as computer readable media, hardware, etc.

Notwithstanding, to expedite prosecution, Applicants have amended claim 17 to recite that the article of manufacture comprises a device implementing code to perform the claimed operations. The Specification discloses this requirement in para. [0021] on pgs. 8-9, which mentions that the "article of manufacture" may comprise devices such as computer readable medium, hardware devices, etc.

The Examiner further found that claim 17 is indefinite because it defines "article of manufacture" as code. Applicants traverse with respect to the amended claims which recites that the article of manufacture comprises a device implementing the code. Applicants note that Specification states that the article of manufacture refers to:

> code or logic implemented in hardware logic (e.g., an integrated circuit chip, Programmable Gate Array (PGA), Application Specific Integrated Circuit (ASIC), etc.)

> or a computer readable medium, such as magnetic storage medium (e.g., hard disk drives, floppy disks,, tape, etc.), optical storage (CD-ROMs, optical disks, etc.), volatile and non-volatile memory devices (e.g., EEPROMs, ROMs, PROMs, RAMs, DRAMs, SRAMs, firmware, programmable logic, etc.).

(Specification, pg. 8, lines 23-29)

The Specification further states that "the 'article of manufacture' may comprise the medium in which the code is embodied", which "may comprise a combination of hardware and software components in which the code is embodied. (Specification, pg. 9, lines 5-8) Thus, the Specification does not define "article of manufacture" as an algorithm or procedure, but instead the implementation of the code or logic in hardware (e.g., an integrated circuit, PGA, ASIC) or a computer readable medium (e.g., disks, optical storage, memory devices, etc). (Specification, pg. 8, lines 23-29).

Applicants submit that the amended claims are definite in reciting that the "article of manufacture" comprises a "device" implementing the code.

2. Claims 1, 2, 9-16, 17, and 19 are Patentable Over the Cited Krishnaiyer

The Examiner rejected claims 1, 2, 9-16, 17, and 19 as anticipated (35 U.S.C. §102(e)) by Krishnaiyer (U.S. Patent App. Pub. No. 2004/0123041).

Claims 1, 9, and 17 require processing a prefetch command indicating at least one conditional statement indicating a condition with respect to content of a received Input/Output (I/O) request and at least one block to prefetch from storage to cache in response to determining that the conditional statement is satisfied.

Applicants amended these claims to recite that the conditional statement indicates a condition with respect to content of a received I/O request. This added requirement is disclosed in at least para. [0011], pg. 4 of the Specification.

The Examiner cited paras. [0024]-[0029] of Krishnaiyer as disclosing the requirements of these claims. (Office Action, pgs. 3-4) Applicants traverse.

The cited paras. [0024-0029] discuss adaptive prefetching code having a loop such that if a condition determines that there is data to prefetch (para. [0024]), then fields of data are prefetched (para. [0025]).

Although the cited Krishnaiyer discusses prefetching if a condition is satisfied, the condition mentions is that there is data to prefetch. Nowhere does the cited Krishnaiyer anywhere disclose the claim requirement of a prefetch command having a conditional statement indicating a condition with respect to the content of a received I/O request. Instead, the condition mentioned in the cited paras. [0024-0029] is independent of the content of the received I/O request and is instead based on whether there is data to prefetch.

Accordingly, claims 1, 9, and 17 are patentable over the cited art because the cited Krishnaiyer does not disclose all the claim requirements.

Claims 2, 10, and 18 are patentable over the cited Krishnaiyer because they depend from claims 1 and 9, respectively, which are patentable over the cited art for the reasons discussed above. Moreover, these claims provide additional grounds of patentability over the cited Krishnaiyer for the following reasons.

Claims 2, 10, and 18 recite that the conditional statement indicates a block that when accessed causes the prefetching of the at least one block to prefetch indicated in the conditional statement, wherein processing the prefetch command comprises generating the prefetch command using predictive analysis techniques to determine blocks anticipated to be accessed if a specified block is accessed, wherein the conditional statements specifies to prefetch the at least one block anticipated to be accessed if the specified block is accessed.

As discussed, the cited paras. [0024-0029] mention conditional prefetch code such that if the condition determines there is data to prefetch, then data is prefetched. However, nowhere is there any disclosure in the cited paras. [0024-0029] of the claim requirement that the condition indicates a block that when accessed causes the prefetching of the at least one block indicated in the conditional statement. Instead, the condition mentioned in the cited . [0024-0029] determines if there is a data prefetch. This cited condition does not disclose the claimed condition of a block accessed in the I/O request that causes the prefetching of the blocks also indicated in the prefetch command..

Accordingly, claims 2 and 10 are patentable over the cited Krishnaiyer because the cited Krishnaiyer does not disclose all the claim requirements. Moreover, claim 18 is distinguished over the cited Krishnaiyer for the reasons discussed with respect to claims 2 and 10 because claim 18 substantially includes the requirements of claims 2 and 10 in "article of manufacture" form.

Amended claim 19 is patentable over the cited Krishnaiyer because it depends from claim 17, which is patentable over the cited art for the reasons discussed above. Moreover, claim 10 provides additional grounds of patentability over the cited Krishnaiyer for the following reasons.

Claim 19 recites that one conditional statements is satisfied if an Input/Output request is directed to a specified block in the conditional statement.

As discussed, the cited paras. [0024-0029] discuss conditional prefetch code that if the condition determines if there is a data prefetch, then fields are prefetched. However, nowhere is there any disclosure in the cited paras. [0024-0029] of the claim requirement that the condition is satisfied if the I/O request is directed to the block specified in the conditional statement. Instead, the condition mentioned in the cited . [0024-0029] determines if there is a data prefetch. This cited condition does not disclose the claimed condition of the I/O request being directed to a specified block in the conditional statement.

Accordingly, claim 19 is patentable over the cited Krishnaiyer because the cited Krishnaiyer does not disclose all the claim requirements. Moreover, claims 3 and 11 are distinguished over the cited Krishnaiyer for the reasons discussed with respect to claim 19 because claims 3 and 11 substantially include the requirements of claim 19 in "method" and "system" form, respectively.

3. Claims 1, 9, and 17 are Patentable Over the Cited Ikeuchi

The Examiner rejected claims 1, 2, 9, 10, 17, and 19 as anticipated (35 U.S.C. §102(e)) by Ikeuchi (U.S. Patent App. Pub. No. 2004/0230742).

With respect to claims 1, 9, and 17, the Examiner cited steps 100, 102, 104, and 106 in FIG. 21 and FIG. 18 of Ikeuchi as disclosing the requirements of these claims. (Office Action, pg. 4) Applicants traverse.

The cited steps of FIG. 21 mentions that if pre-fetch of the virtual disk is necessary, then a judgment is made whether requesting a prefetch is possible by a judgment condition based on the number of requests in process. (Ikeuchi, paras. [0174-0175], pg. 9). Ikeuchi mentions that determining whether prefetches are possible is based on the load of host I/Os and internal I/Os, (prefetches and write backs) to manage the number of processing requests to the virtual disk. (Ikeuchi, para. [0134], pg. 7).

Nowhere do the cited steps of FIG. 21 anywhere disclose that a prefetch command indicates a conditional statement and a block to prefetch if the condition is satisfied. The cited Ikeuchi discusses a condition on a prefetch based on the number of processing requests pending against the virtual disk. Although this cited condition may limit prefetch operations, nowhere do the cited steps disclose that a prefetch command itself indicates a conditional statement. Instead, the cited condition of Ikeuchi is independent of any prefetch command and is instead based on a Dynamic Traffic Control (DTC) module managing the load of requests against the virtual disk. See, para. [0134].

Moreover, the cited Ikeuchi nowhere discloses that the conditional statement indicates a condition with respect to content of a received Input/Output request. Instead, the cited Ikeuchi discusses a condition based on the number of processing requests pending, not the content of a received I/O request as claimed.

Further, the cited Ikeuchi nowhere discloses that a prefetch command indicates a block to prefetch if the condition is satisfied. Instead, Ikeuchi provides a condition to limit prefetching in based on the load against the virtual disk.

The cited FIG. 18 shows a block diagram of modules, such as a cache control module having a module 34-3 for requesting a prefetch due to a read request. See, Ikeuchi, para. [00151], pg. 8.

Although FIG. 18 shows a module for requesting a prefetch request, nowhere does this cited FIG. 18 anywhere disclose that a prefetch command has a conditional statement indicating a condition with respect to content of a received Input/Output request and a block to prefetch if the condition is satisfied.

Accordingly, claims 1, 9, and 17 are patentable over the cited Ikeuchi because the cited Ikeuchi does not disclose all the claim requirements.

4. Claims 1-24 are Patentable Over the Cited Lange

The Examiner rejected claims 1-24 as anticipated (35 U.S.C. §102(e)) by Lange (U.S. Patent App. Pub. No. 2005/0198439).

With respect to claims 1, 9, and 17, the Examiner cited blocks 540, 550, and 560 of FIG. 5 of Lange. (Office Action, pg. 4) FIG. 5 provides a method for prefetching data. Lange

mentions that a new prefetch sequence begins if a cache miss is detected, i.e., the requested data is not in cache. (Lange, paras. [0063-0064], pgs. 5-6)

Nowhere do the cited steps of Lange anywhere disclose that a prefetch command indicates a conditional statement and a block to prefetch if the condition is satisfied. The cited Lange mentions that a prefetch occurs if there is a cache miss, but nowhere discloses that a prefetch command itself indicates a conditional statement. Instead, the cited condition of Lange is independent of any prefetch command and is instead based on whether or not there is a cache miss.

Moreover, the cited Lange nowhere discloses that the conditional statement indicates a condition with respect to content of a received I/O request. Instead, the cited Lange discusses a condition based on whether there is a cache miss (the requested data is in cache), which is independent of a condition with respect to the content of the received I/O request.

Further, the Examiner has not cited any part of Lange that discloses that a prefetch command indicates a block to prefetch if the condition is satisfied.

Accordingly, claims 1, 9, and 17 are patentable over the cited Lange because the cited Lange does not disclose all the claim requirements.

Claims 2-8, 10-16, and 18-24 are patentable over the cited art because they depend from one of claims 1, 9, and 17, which are patentable over the cited art for the reasons discussed above. Moreover, the following dependent claims provide additional grounds of patentability over the cited art.

Claims 2, 10, and 18 depend from claims 1, 9, and 17 and further require that the conditional statement indicates a block that when accessed causes the prefetching of the at least one block to prefetch indicated in the conditional statement and that processing the prefetch command comprises generating the prefetch command using predictive analysis techniques to determine blocks anticipated to be accessed if a specified block is accessed, wherein the conditional statements specifies to prefetch the at least one block anticipated to be accessed if the specified block is accessed.

The Examiner cited FIGs. 5, 6 and paras. [0064-0065] of Lange as disclosing the additional requirements of these claims. (Office Action, pg. 5) Applicants traverse.

The cited paras. [0064-0065] mention that a prefetch is performed if there is a cache miss and that a current prefetch sequence may be ended when a new cache miss occurs. FIG. 6 is a flowchart of a method for retrieving a sequence of data items from a main memory.

Nowhere does the cited Lange disclose the claim requirement that the condition indicates a block that when accessed causes the prefetching of the at least one block to prefetch indicated in the conditional statement. Instead, the cited Lange mentions that prefetching occurs upon a cache miss. The Examiner has not cited any part of Lange that discloses that a prefetch command conditional statement indicates a block, such that prefetching is performed when the I/O request accesses the indicated block.

Accordingly, claims 2, 10, and 18 are patentable over the cited Krishnaiyer because the cited Krishnaiyer does not disclose all the claim requirements.

Claims 3, 11, and 19 depend from claims 1, 9, and 17 and further recite that the condition with respect to the I/O request comprises a specified block, wherein one conditional statement is satisfied if the received I/O request is directed to the specified block indicated in the condition of the conditional statement.

The cited para. [0064] mentions that a prefetch occurs if there is a cache miss, i.e., the requested data is not in cache. However, nowhere is there any disclosure in the cited Lange of the claim requirement that the condition is satisfied if the I/O request is directed to the block specified in the conditional statement. Instead, the condition mentioned in the cited Lange concerns whether the requested data is in cache, i.e., a cache hit or miss, not whether the I/O request is directed to a specified block indicated in the conditional statement of the prefetch command. There is no disclosure in the cited Lange of a prefetch command indicating a specified block such that prefetch occurs if the I/O request is directed to the block specified in the condition.

Accordingly, claims 3, 11, and 19 are patentable over the cited Lange because the cited Lange does not disclose the additional requirements of these claims.

Claim 5, 13, and 21 depend from claims 3, 11, and 19 and further recite that processing the prefetch command further comprises including a duration parameter in the prefetch command indicating a duration of the prefetch command.

The Examiner found that a duration was implicit because the prefetch command lasts for a specified duration of one page or pages or until the buffer is full. (Office Action, pg. 6). Applicants traverse.

Although a prefetch operation may have an implicit duration and ends at a point-in-time, the Examiner has not cited any part of Lange that discloses that a prefetch command includes a duration parameter indicating the duration of the command. Applicant submits that an implicit duration does not disclose the claim requirement of including a duration of the prefetch command within the prefetch command.

Accordingly, claims 5, 13, and 21 are patentable over the cited Lange because the cited Lange does not disclose the additional requirements of these claims.

Claims 6, 14, and 22 depend from claims 1, 9, and 17, respectively, and further recite that processing the prefetch command comprises receiving the prefetch command and further performing: receiving an Input/Output request directed to a target block; determining whether the target block satisfies the conditional statement of one prefetch command; and prefetching the at least one block to prefetch indicated in the conditional statement of one prefetch command into the cache in response to determining that the target block satisfies the conditional statement of one prefetch command.

The Examiner cited para. [0042] and FIGs. 5 and 6 of Lange with respect to the additional requirements of these claims. (Office Action, pgs. 5-6) Applicants traverse.

The cited para. [0042] mentions a direction selector that establishes an access direction of memory accesses when a cache miss is detected. When a cache hit occurs, i.e., the requested data is in cache, it may be undesirable to interrupt the current prefetch sequence. Lange mentions that selecting the direction only when a cache miss is detected is useful.

Nowhere does the cited para. [0042] anywhere disclose that a determination is made as to whether a target block of an I/O request satisfies a conditional statement of one prefetch command. Instead, the cited para. [0042] discusses determining the direction of memory access. Further, the cited Lange provides for prefetching upon a cache miss, i.e., when the requested data is not in cache. Nowhere does the cited Lange disclose that prefetching occurs when the target block satisfies a conditional statement of one prefetch command. Instead, the cited Lange prefetches if there is a cache miss, not based on whether the target block satisfies a conditional statement indicated in a prefetch command.

Accordingly, claims 6, 14, and 22 are patentable over the cited Lange because the cited Lange does not disclose the additional requirements of these claims.

Claims 7, 15, and 23 depend from claims 6, 14, and 22 and further require that determining whether the target block satisfies the conditional statement of one prefetch command comprises determining whether the target block satisfies the conditional statement of one unexpired prefetch command.

The Examiner cited the above discussed steps 540 and 560 of FIG. 5 as disclosing the additional requirements of these claims. (Office Action, pg. 6) Applicants traverse.

As discussed, the cited steps 540 and 560 mention that prefetch begins if there is a cache miss, i.e., the requested data is not in the cache. Nowhere does the cited Lange disclose determining whether the target block satisfies the conditional statement of one unexpired prefetch command. The cited Lange does not disclose that a prefetch command expires. Although a prefetch operation may end, nowhere does the cited Lange disclose that a prefetch command specifying a conditional statement related to the content of an I/O request expires. Moreover, the only condition concerned in Lange to determine whether to perform a prefetch is if the requested data is not in cache, i.e., a cache miss. Nowhere does the cited Lange determine whether a target block satisfies a conditional statement of an unexpired prefetch command.

Accordingly, claims 7, 15, and 23 are patentable over the cited Lange because the cited Lange does not disclose the additional requirements of these claims.

Claims 8, 16, and 24 depend from claims 1, 9, and 17 and further recite that one conditional statement includes a plurality of branch conditions, wherein each branch condition indicates one block and is associated with at least one block to prefetch, further comprising: prefetching all blocks to prefetch associated with the branch conditions in the conditional statement; and removing blocks to prefetch from cache associated with branch conditions that are not satisfied in response to determining that the block indicated in one branch condition is accessed.

The Examiner cited steps from FIGs. 5 and 6 as disclosing the requirements of these claims. (Office Action, pgs. 6-7) Applicants traverse.

As discussed, the cited FIGs. 5 and 6 discuss prefetching if requested data is not in cache, i.e., a cache miss and determining a direction of access of reading the data to retrieve a sequence of data items from the memory. The steps 600-640 discuss prefetching data in sequence, and

that a determination is made as to whether to continue with the current prefetch sequence or begin a new prefetch sequence.

Nowhere does the cited Lange disclose prefetching all blocks associated with branch conditions. Instead, the cited step 640 of Lange mentions that a determination is made whether to continue with the current prefetch sequence, and if so, continue prefetching. Nowhere does Lange disclose prefetching all blocks associated with conditions and then removing blocks to prefetch associated with branch conditions that are not satisfied. Instead, the cited Lange only prefetches if the condition of step 640 is satisfied. The Examiner has not cited any part of Lange that first prefetches data associated with conditions, and then removes data associated with conditions not satisfied.

The Examiner cited paras. [0043] and [0064], finding that data prefetched is replaced with newly prefetched data. Although Lange may have previously prefetched data replaced with newly prefetched data, nowhere does Lange disclose removing prefetched data associated with conditions of prefetch commands that are not satisfied. Instead, the cited Lange removes data as a result of overwriting, not based on the claim requirement of whether conditions are satisfied.

Accordingly, claims 8, 16, and 24 are patentable over the cited Lange because the cited Lange does not disclose the additional requirements of these claims.

5. Added claim 25 is Patentable Over the Cited Art

Added claim 25 depends from claim 17 and further recites that the device comprises at least one of a computer readable medium including the code, wherein a processor executes the code in the computer readable medium to cause the operations to be performed, and a hardware device implementing the code as hardware logic that when executed causes the operations to be performed.

The additional requirements of claim 25 are disclosed in at least para. [0021] on pgs. 8-9 of the Specification.

Applicants submit that claim 25 is patentable over the cited art because it depends from claim 17, which is patentable over the cited art for the reasons discussed above.

Conclusion

For all the above reasons, Applicants submit that the pending claims 1-25 are patentable over the art of record. Applicants submit herewith the fee for the added claim. Nonetheless, should any additional fees be required, please charge Deposit Account No. 09-0449.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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